CLAIMS

We claim:

1. A method for verifying core determinacy, the method comprising:

extracting data stored in core model structures;

comparing the extracted data of one modeled processor core with extracted data of another modeled processor core;

determining if any mismatching data will cause core divergence; and

facilitating notice of an error if any mismatching data will cause core divergence.

2. The method of claim 1, wherein extracting data comprises extracting data from core data storage and interconnect elements.

3. The method of claim 2, wherein extracting data comprises extracting data from at least one of core buffers, core caches, core queues, core state variables, core state machines, and bus values.

4. The method of claim 1, wherein determining comprises accessing a data structure that matches divergence results with given mismatched data.

5. The method of claim 1, wherein determining comprises implementing an algorithm that uses the mismatched data as inputs.

6. The method of claim 1, wherein facilitating notice comprises pending a check for a lockstep block checker to signal when divergence occurs.

7. The method of claim 6, wherein facilitating notice comprises flagging an error if the lockstep block checker does not signal that divergence occurred.

8. The method of claim 1, further comprising determining if a modeled processor is operating in lockstep mode.

9. The method of claim 8, wherein determining if a modeled processor is operating in lockstep mode comprises analyzing at least one of a lockstep block and a lockstep block checker.

10. A system for verifying core determinacy, the system comprising:

means for determining if a modeled processor is operating in a lockstep mode;

means for extracting data stored in core model structures;

means for comparing the extracted data to determine if any data associated with one processor core does not match data associated with another processor core; and

means for determining if any mismatching data will cause core divergence.

11. The system of claim 10, wherein the means for determining if a modeled processor is operating in a lockstep mode comprise means for analyzing at least one of a lockstep block and a lockstep block checker.

12. The system of claim 10, wherein the means for extracting data comprise means for extracting data from core data storage and interconnect elements.

13. The system of claim 10, wherein the means for determining if any mismatching data will cause core divergence comprise at least one of a data structure and an algorithm.

14. The system of claim 10, further comprising means for pending a check for a lockstep block checker to signal when divergence occurs.

15. The system of claim 10, further comprising means for flagging an error.

16. A determinacy checker stored on a computer-readable medium, the system comprising:

logic configured to determine if a modeled processor is operating in a lockstep mode;

logic configured to extract data stored in core model structures;

logic configured to compare the extracted data;

logic configured to determine if any data associated with one processor core does not match data associated with another processor core;

logic configured to determine if any mismatching data will cause core divergence; and

logic configured to facilitate notification of an error if any mismatching data will cause core divergence.

17. The checker of claim 16, wherein the logic configured to determine if a modeled processor is operating in a lockstep mode comprises logic configured to analyze at least one of a lockstep block and a lockstep block checker.

18. The checker of claim 16, wherein the logic configured to extract data comprises logic configured to extract data from core data storage and interconnect elements.

19. The checker of claim 16, wherein the logic configured to determine if any mismatching data will cause core divergence comprises logic configured to access at least one of a data structure that matches divergence results with given mismatched data and an algorithm that uses the mismatched data as inputs.

20. The checker of claim 16, wherein the logic configured to facilitate notification comprises logic configured to pend a check for a lockstep block checker to signal when divergence occurs.

21. The checker of claim 16, wherein the logic configured to facilitate notification comprises logic configured to flag an error.

22. A computer system, comprising:

a processing device; and

memory including a determinacy checker that is configured to extract data stored in core model structures, compare the extracted data, determine if any mismatching data will cause core divergence, and facilitate notification of an error if the mismatching data will cause core divergence.

23. The system of claim 22, wherein the checker is configured to extract data from core data storage and interconnect elements.

24. The system of claim 22, wherein the checker is configured to pend a check for a lockstep block checker to signal when divergence occurs.

25. The system of claim 22, wherein the checker is configured to flag an error.